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JC962 U.S. PTO 11/28/00

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PTO/SB/05 (12/97)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	TI-29632
First Named Inventor or Application Identifier	U-Ming Ko
Title	Input/Output Architecture For Integrated Circuits
Express Mail Label No.	EL547744331US

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

JC564 U.S. PTO 09/723563 11/28/00

1. [X] *Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification *[Total Pages 20]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC d113)* *[Total Sheets 6]*
4. Oath or Declaration *[Total Pages 1]*
   - a. [X] Newly Executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR §1 63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3 73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

☐Continuation ☐Divisional ☐Continuation-in-part (CIP) of prior application No: / .

Prior application information: ***Examiner*** ***Group / Art Unit:***

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No or Attach bar code label here)* or [X] *Correspondence address below*

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Signature	Ronald O. Neerings	Date	11/28/00

Burden Hour Statement: This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

PTO/SB/17 (1/98)
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FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT	($) 1,248.00

Complete If Known	
Application Number	TBD
Filing Date	11/28/2000
First Named Inventor	U-Ming Ko
Examiner Name	TBD
Group / Art Unit	TBD
Attorney Docket No.	TI-29632

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge to the following Deposit Account.

Deposit Account Number: 20-0668

Deposit Account Name: Texas Instruments Incorporated

☐ Charge any additional fee required or credit any overpayment

☒ Charge all indicated fees and any additional fee required or credit any overpayment

2. ☐ **Payment Enclosed:**

☐ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	$710
106	330	206	165	Design filing fee	$
107	540	207	270	Plant filing fee	$
108	790	208	395	Reissue filing fee	$
114	150	214	75	Provisional filing fee	$

SUBTOTAL (1) ($)710

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	=	Fee Paid
Total Claims	41	-20**=	21	x	18	=	378
Independent Claims	5	-3** =	2	x	80	=	160
Multiple Dependent					0	=	0

**or number previously paid, if greater, For Reissue, see below

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent Claims in excess of 3
104	270	204	135	Multiple dependent claims in excess of 3
109	82	209	41	**Reissue independent claims over original patent
110	22	210	11	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)538

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Fee Code	Entity Fee ($)	Small Fee Code	Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension of time within second month	
117	950	217	475	Extension of time within third month	
118	1,510	218	755	Extension of time within fourth month	
128	2,060	228	1,030	Extension of time within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a pubic use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per properly (time number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Ronald O. Neerings			Reg Number	34,227
Signature	Ronald O. Neerings	Date	11/28/00	Deposit Account User ID	

INPUT/OUTPUT ARCHITECTURE FOR INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to the field of integrated circuit layout and design. More specifically, the present invention relates to a design process and structure for providing input/output components on an integrated circuit.

Description of the Related Art

The development of the technology for the fabrication and design of integrated circuits has allowed designers to place ever increasing functionality onto a smaller area of integrated circuits. This makes the surface area of an integrated circuit extremely valuable. A component of integrated circuits that occupies a relatively large area are the input/output (I/O) modules.

I/O Modules provide the attachment point for electrical bonding to the integrated circuit die. I/O modules generally consist of a bond pad, an electrostatic discharge protection device and I/O buffer circuitry. The core circuitry is generally composed of very small devices. These devices are fast and densely packed, but fragile. The I/O modules provide protection to the core circuitry as well as a connection point for getting

signals on and off of the integrated circuit. Because they must provide this protection function, I/O modules use relatively large devices and occupy a disproportionate area on the integrated circuit die.

I/O modules are generally positioned on the periphery of the integrated circuit die. This makes the process of bonding to the bond pads easier and helps buffer the core circuitry from the physical stresses of cutting the die from the semiconductor wafer during manufacturing. The area occupied by the I/O modules is determined by the height (distance from the edge of the die to interior edge of the I/O modules) of the I/O modules. The remaining portion of the chip is available for core circuitry. Designers are always looking for ways to put more functionality onto an integrated circuit. Because of this, it is desirable to use the minimum area necessary for I/O modules to provide as much area as possible for the core circuitry.

BRIEF SUMMARY OF THE INVENTION

It is an object of the present invention to provide a structure and method allowing the positioning of integrated circuit elements efficiently.

It is a further object of the present invention to minimize the area necessary for the I/O periphery in an integrated circuit.

These and other objects are provided by a described embodiment of the present invention, which includes an integrated circuit having a plurality of I/O modules. The I/O modules include a bond pad formed on a substrate. The I/O modules also include an electrostatic discharge device formed in the substrate. The electrostatic discharge device is at least partially formed beneath the bond pad. The I/O module also includes an I/O buffer formed in the substrate. The I/O buffer is connected to the bond pad. The I/O buffer provides communication between the bond pad and circuitry formed in the substrate. The circuitry is positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference should be made to the following Detailed Description taken in connection with the accompanying drawings in which:

Figure 1 is a layout diagram of a prior art I/O module;

Figure 2 is a layout diagram of the I/O module of Figure 1 positioned on an integrated circuit die;

Figure 3 is a layout diagram showing a plurality of prior art I/O modules positioned next to a functional core;

Figure 4 is a layout diagram of an embodiment of the present invention;

Figure 5 is a layout diagram another embodiment of the present invention in which a plurality of I/O modules positioned by a functional core;

Figure 6 is a chart showing the die area recovered using the described embodiments of the present invention;

Figure 7 is a detailed layout diagram of the embodiment of Figure 4;

Figure 8 is a schematic diagram of an output circuit suitable for used with the described embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 is a layout diagram of a prior art I/O module. I/O module 10 includes a bond pad 12, electrostatic discharge (ESD) device 14 and I/O buffer 16. Also included in Figure 1 are scribe area 20 and scribe seal 22. Scribe area 20 provides space for the saw that separates a wafer into die. Scribe seal 22 is a physical buffer area between the dice and the scribe area. Scribe seal allows for the dissipation of physical stress during the dicing process.

The components of I/O module 10 are laid out in the conventional manner with the bond pad and the edge of the integrated circuit die and the I/O buffer 16 positioned between the functional core 40 and bond pad 12. I/O module 10 is an advanced module in that ESD device 14 is positioned beside bond pad 12.

Figure 2 is a layout diagram showing the position of I/O modules 10 on die 30 in I/O region 32. Functional core 40 is surrounded by I/O region 32. The overall size of the die 30 is determined by the width of core 40 (X) plus twice the height of the I/O modules 10 times the length of core 40 (Y) plus twice the height of the I/O modules 10. The formula for the area is

$$\text{Area} = (X+2H)*(Y+2H)$$

which can be written as

$$Area = XY+2HY+2HX +4H^2.$$

As can be seen from the above formula, the height of the I/O modules 10 has a large impact on the overall area of the die 30. Although Figure 2 includes fourteen I/O modules 10, it is more common for an integrated circuit to include from 64 to 300 I/O modules. Figure 3 is an enlarged portion of the layout of Figure 2 showing four I/O modules 10 and their position relative to functional core 40.

Figure 4 is a layout diagram of a novel I/O module 100, which is structured according to the teachings of the present invention. I/O module 100 is preferably formed on a crystalline semiconductor substrate. Bond pad 112 is positioned adjacent to scribe seal 122 as in the I/O module 10 of Figure 1. Bond pad 112 is preferably formed of an aluminum composite layer, copper layer or gold clad copper layer having conductive upper surface for ball bonding. I/O buffer 116 is a similar I/O buffer circuit with a similar layout to that of I/O buffer 16. However, because I/O buffer 116 is positioned adjacent to scribe seal 122, the overall height Z of I/O module 100 is the height of I/O buffer 116 plus the width of scribe seal 122 and one half of scribe line 120.

In contrast, the height H of prior art I/O Module is height of I/O buffer 16 plus the height of ESD device 14 plus the width of scribe seal 22 and one half of scribe line 20. For example, the height of I/O buffer 16 may be 71μ, the height of ESD device 14 may be 21μ, the height of bond pad 12 may be 50μ and the combined height of the scribe seal 22, scribe line 20 and additional spacing may be 46μ. This provides an overall height H of 188μ.

The inventive I/O module 100, however, provides a much smaller height Z using the same design rules. With the same dimensions for components of I/O module 10, I/O module 100 has a height of 81μ for I/O module 116 plus 46μ for scribe line 120 and scribe seal 122. By careful layout of I/O module 116, its height can be reduced to 74μ, thus providing an overall height Z of 120μ.

Figure 5 shows I/O modules 100 as positioned adjacent to functional core 40. Functional core 40 may be any function capable of being implemented with integrated circuitry. For example, functional core 40 may comprise an application specific integrated circuit or a digital signal processor. Preferably, the circuitry of functional core 40 is fabricated using CMOS or BiCMOS processes. Because I/O modules 100 are wider than corresponding prior art modules, fewer I/O modules 100

can be provided for a given size of functional core 40. However, integrated circuit designs are rarely constrained by the number of I/O buffers. More often, the number of input/output connections is limited by the package. Packages that provide more that 200 connection points (for advanced ball grid arrays) can be cost prohibitive. Therefore, I/O modules 100 significantly reduce the die size for a given functionality without constraining the operational characteristics of the integrated circuit. Conversely, I/O modules 100 allow for a larger functional core for a given die size.

Figure 6 is a chart comparing the die size and wasted area using the prior art I/O module. Six functional core sizes are listed. For each core size, a prior art I/O module with height H is listed and a corresponding novel module with the height Z is listed. Also listed is the total area using each module, the maximum number of I/O modules that can be placed on the die, the wasted area and the percentage of area wasted using the prior art. As can be seen from Figure 6, the novel I/O module 100 reduces wasted space by 6%-13%, depending on functional core size.

Figure 7 is a layout diagram showing the specific topographical features of I/O module 100. ESD device 114

can be any number of electrostatic discharge devices. Examples of suitable devices can be found in Chen et al., U.S. Patent No. 5,982,217, which is assigned to the assignee of this application and which is incorporated herein by reference.

I/O buffer 116 can be any number of known designs for providing input and output drivers. An example is shown in Figure 8. I/O buffer 116 is preferably fabricated using a multi-level metal system and a device fabrication process such as that shown in Smayling et al., U.S. Patent No. 5,767,551, which is assigned to the assignee of this application and which is hereby incorporated by reference. I/O buffer 116 is a three stage, complementary output buffer designed for high speed and to provide a well conditioned output signal.

The input signal on input A of I/O buffer 116 is inverted by transistor 202 and a push-pull inverter formed by transistors 204 and 206. Transistor 208 prevents saturation of transistor 206 for high speed operation. The output from transistors 204 and 206 is inverted again by transistors 210 and 212 with a pull up (when appropriate) from transistor 214. The drain of transistor 214 is connected to the high V_{DD} voltage supply (symbolized by a circle). The output from transistors

204 and 206 also drives the push-pull inverter formed by transistors 216 and 218. The output from transistors 210 and 212 drives the gate of drive transistor 220. The output from transistors 216 and 218 drives the gate of drive transistor 222. The output from transistors 210 and 212 also drives the gate of pull-up transistor 224.

The inverse of input A, A' is applied to the gates of transistors 226, 228 and 230. Transistors 226, 228, 230, 232, 234, 236, 238, 240, 242 and 244 provide the same functions as transistors 202, 204, 206, 208, 214, 210, 212, 216, 218, and 224, respectively. Additionally, transistors 245 and 248 invert and delay the output of transistors 236 and 238. In addition, transistors 250 and 252 invert and delay the output of transistors 240 and 242. The output of transistors 236 and 238 drives the gate of output transistor 254. The output of transistors 250 and 252 are used to drive the gate of output transistor 256.

Transistors 258, 260, 262, 264 and 266 constitute a pull down AND gate driving output transistor 278. Transistors 268, 270, 272, 274 and 276 constitute a pull-down AND gate driving output transistor 280. The pull-down portions of the gates are voltage limited by transistors 262 and 272 in that are gate strapped to V_{DD}

(the lower voltage supply symbolized by a horizontal line). This prevents saturation of transistors 278 and 280. The parallel pull-up transistors 258, 260, 268 and 270 provide rapid shut off of transistors 278 and 280. The gate inputs of transistors 258-270 are timed to provide staggered gate charging or draining capacity and to avoid race conditions where all transistors in a series are on.

Transistors 282-290 provide a complementary pull-up function for output transistors 298 and 300 to the function provided by transistors 258-270 for output transistors 278 and 280. In summary, transistors 220, 222, 254 and 256 provide rapid medium drive signals to begin and signal transition. Transistors 278, 280, 298 and 300 provide high capacity drive with gate drive signals that are carefully controlled. I/O buffer 116 in Figure 8 is an output buffer of a certain preferred structure. However, the structure of Figure 8 in no way limits the intended scope of the invention. The invention contemplates the use of any input or output buffer.

Although specific embodiments of the present invention are described herein, they are not to be construed as limiting the scope of the invention. For

example, although specific circuits and device fabrication techniques are described and referred to herein, many specific devices and fabrication techniques may be advantageously used within the scope of the invention. Many embodiments of the invention will become apparent to those skilled in the art in light of the teachings of this specification. The scope of the invention is only limited by the claims appended hereto.

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is set forth in the following claims.

CLAIMS

1. An integrated circuit having a plurality of I/O modules comprising:

a bond pad formed on a substrate;

an electrostatic discharge device formed in the substrate, the electrostatic discharge device being at least partially formed beneath the bond pad;

an I/O buffer formed in the substrate and connected to the bond pad, the I/O buffer providing communication between the bond pad and circuitry formed in the substrate, wherein the circuitry is positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer.

2. The integrated circuit of Claim 1 wherein the substrate is a silicon substrate.

3. The integrated circuit of Claim 1 wherein the I/O buffer is an output buffer.

4. The integrated circuit of Claim 1 wherein the I/O buffer is an input buffer.

5. The integrated circuit of Claim 1 wherein the I/O buffer is a complementary output buffer.

6. The integrated circuit of Claim 1 wherein the circuitry is CMOS circuitry.

7. The integrated circuit of Claim 1 wherein the circuitry is BiCMOS circuitry.

8. The integrated circuit of Claim 1 wherein the circuitry is an application specific integrated circuit.

9. The integrated circuit of Claim 1 wherein the circuitry is digital signal processor.

10. The integrated circuit of Claim 1 wherein the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

11. An integrated circuit comprising:

a functional core formed on a substrate, the functional core being positioned centrally on the substrate; and

an I/O region positioned at the periphery of the functional core, the I/O region including a plurality of I/O modules, the I/O modules including:

a bond pad formed on a substrate;

an electrostatic discharge device; and

an I/O buffer wherein the I/O buffer is not positioned between the bond pad and the functional core.

12. The integrated circuit of Claim 11 wherein the substrate is a silicon substrate.

13. The integrated circuit of Claim 11 wherein the I/O buffer is an output buffer.

14. The integrated circuit of Claim 11 wherein the I/O buffer is an input buffer.

15. The integrated circuit of Claim 11 wherein the I/O buffer is a complementary output buffer.

16. The integrated circuit of Claim 11 wherein the functional core is CMOS circuitry.

17. The integrated circuit of Claim 11 wherein the functional core is BiCMOS circuitry.

18. The integrated circuit of Claim 11 wherein the functional core is an application specific integrated circuit.

19. The integrated circuit of Claim 11 wherein the functional core is digital signal processor.

20. The integrated circuit of Claim 11 wherein the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

21. An integrated circuit comprising:

a functional core formed on a substrate, the functional core including a plurality of integrated circuit elements and being positioned centrally on the substrate; and

an I/O region positioned at the periphery of

the functional core, the I/O region including a plurality of I/O modules, the I/O modules including:

a bond pad formed on a substrate, the bond pad including a conductive surface for providing electrical connection to external devices;

an electrostatic discharge device formed beneath the bond pad; and

a CMOS I/O buffer wherein the I/O buffer is not positioned between the bond pad and the functional core.

22. A method for forming an integrated circuit having a plurality of I/O modules comprising:

forming a bond pad formed on a substrate;

forming an electrostatic discharge device formed in the substrate, the electrostatic discharge device being at least partially formed beneath the bond pad; and

forming an I/O buffer formed in the substrate and connected to the bond pad, the I/O buffer providing communication between the bond pad and circuitry formed in the substrate, wherein the circuitry is positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer.

23. The method of Claim 22 wherein the substrate is a silicon substrate.

24. The method of Claim 22 wherein the I/O buffer is an output buffer.

25. The method of Claim 22 wherein the I/O buffer is an input buffer.

26. The method of Claim 22 wherein the I/O buffer is a complementary output buffer.

27. The method of Claim 22 wherein the circuitry is CMOS circuitry.

28. The method of Claim 22 wherein the circuitry is BiCMOS circuitry.

29. The method of Claim 22 wherein the circuitry is an application specific integrated circuit.

30. The method of Claim 22 wherein the circuitry is digital signal processor.

31. The method of Claim 22 wherein the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

32. A method for forming an integrated circuit comprising:

providing a functional core formed on a substrate, the functional core being positioned centrally on the substrate; and

in an I/O region positioned at the periphery of the functional core, forming a plurality of I/O modules, the steps for forming the I/O modules including:

forming a bond pad formed on a substrate;

forming an electrostatic discharge device; and

forming an I/O buffer wherein the I/O buffer is not positioned between the bond pad and the functional core.

33. The method of Claim 32 wherein the substrate is a silicon substrate.

34. The method of Claim 32 wherein the I/O buffer is an output buffer.

35. The method of Claim 32 wherein the I/O buffer is an input buffer.

36. The method of Claim 32 wherein the I/O buffer is a complementary output buffer.

37. The method of Claim 32 wherein the functional core is CMOS circuitry.

38. The method of Claim 32 wherein the functional core is BiCMOS circuitry.

39. The method of Claim 32 wherein the functional core is an application specific integrated circuit.

40. The method of Claim 32 wherein the functional core is digital signal processor.

41. The method of Claim 32 wherein the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

INPUT/OUTPUT ARCHITECTURE FOR INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

A described embodiment of the present invention includes an integrated circuit having a plurality of I/O modules. The I/O modules include a bond pad formed on a substrate. The I/O modules also include an electrostatic discharge device formed in the substrate. The electrostatic discharge device is at least partially formed beneath the bond pad. The I/O module also includes an I/O buffer formed in the substrate. The I/O buffer is connected to the bond pad. The I/O buffer provides communication between the bond pad and circuitry formed in the substrate. The circuitry is positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer.

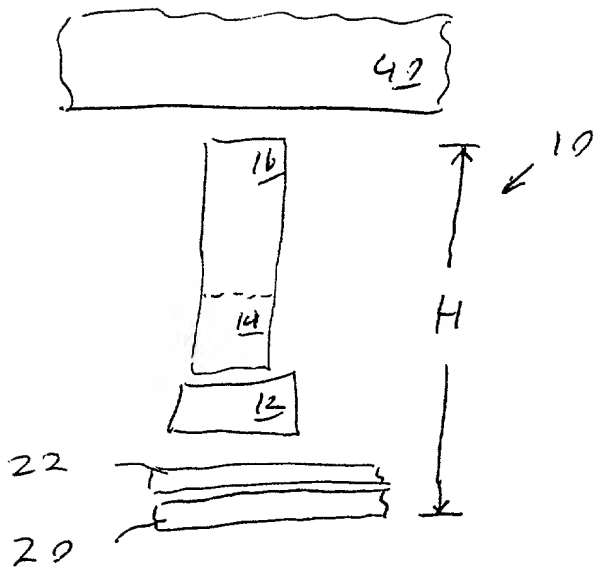

Figure 1 (Prior Art)

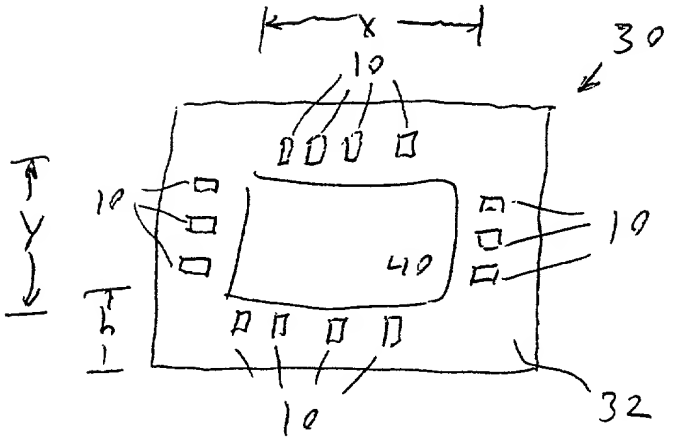

Figure 2 (Prior Art)

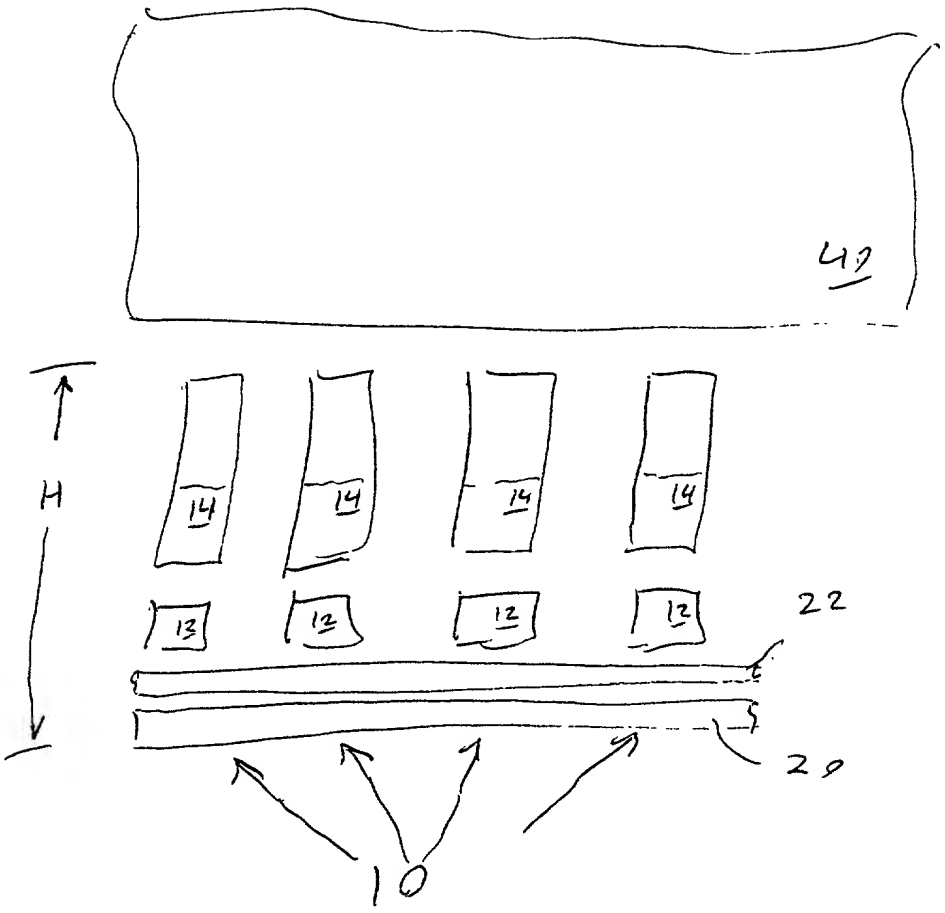

Figure 3 (Prior Art)

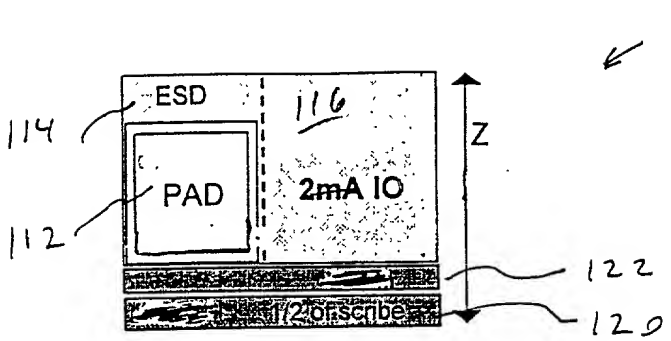

Figure 4

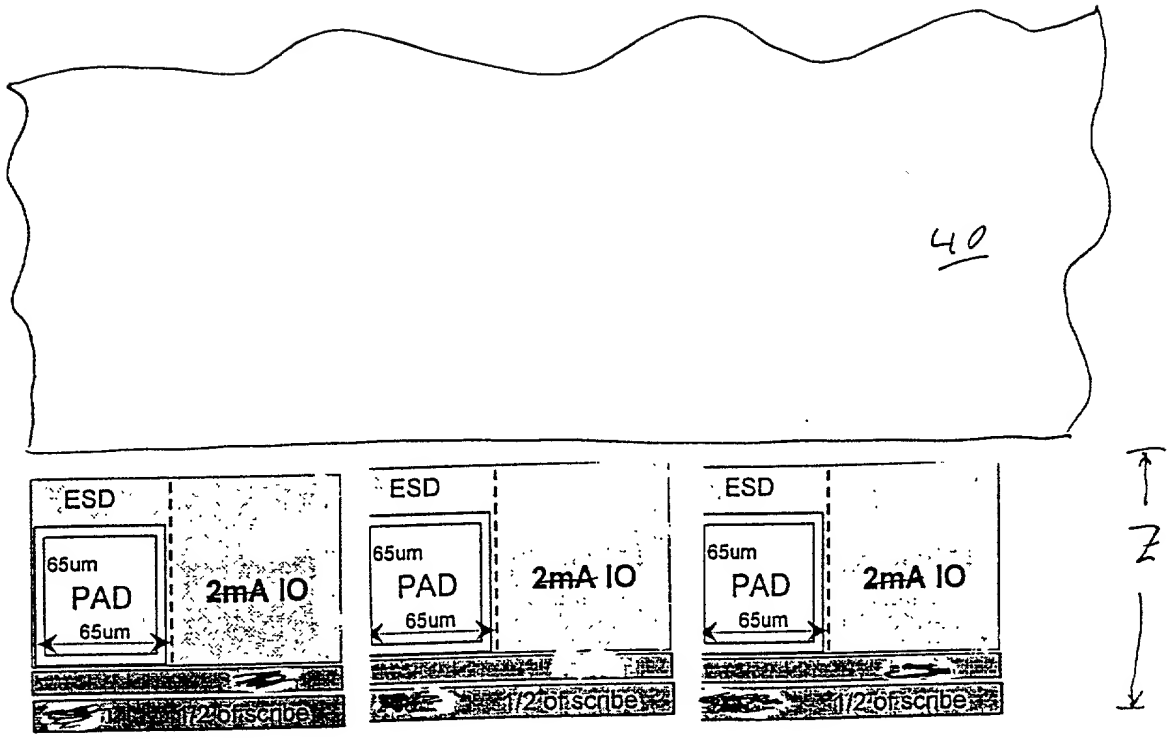

Figure 5

Core area,mm2	mm /side	IO height, um	IO width, um	Area	max IO	wasted area	% of core
10	3.162278	H = 188	75	12.51941	169	1.67	13%
		Z = 120	108	11.57549	117		
20	4.472136	H = 188	75	23.50442	239	2.33	10%
		Z = 120	108	22.20423	166		
30	5.477226	H = 188	75	34.26025	292	2.83	8%
		Z = 120	108	32.68667	203		
40	6.324555	H = 188	75	44.89744	337	3.26	7%
		Z = 120	108	43.09339	234		
50	7.071068	H = 188	75	55.45882	377	3.63	7%
		Z = 120	108	53.45171	262		
60	7.745967	H = 188	75	65.96634	413	3.97	6%
		Z = 120	108	63.77566	287		

Figure 6

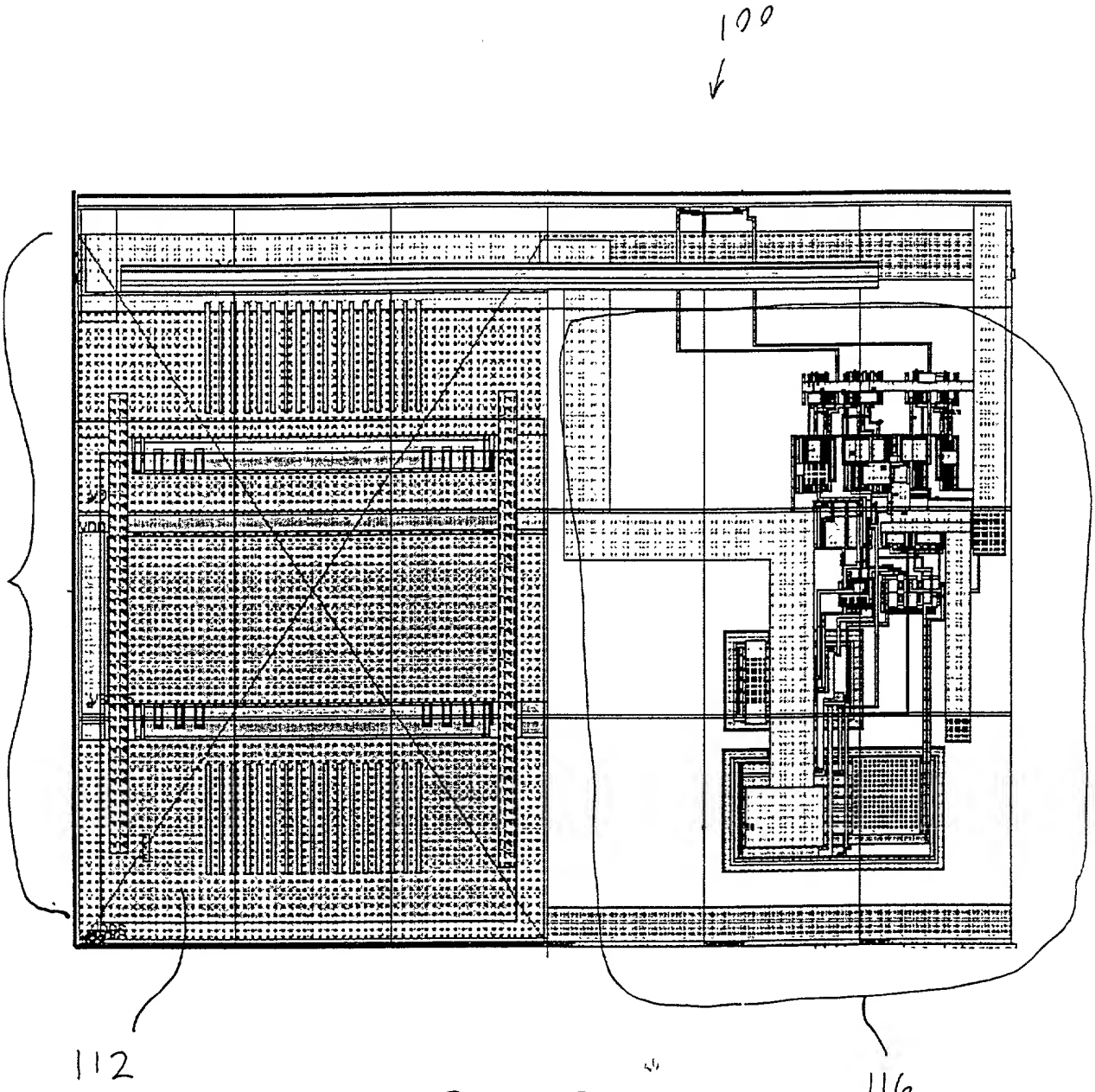

Figure 7

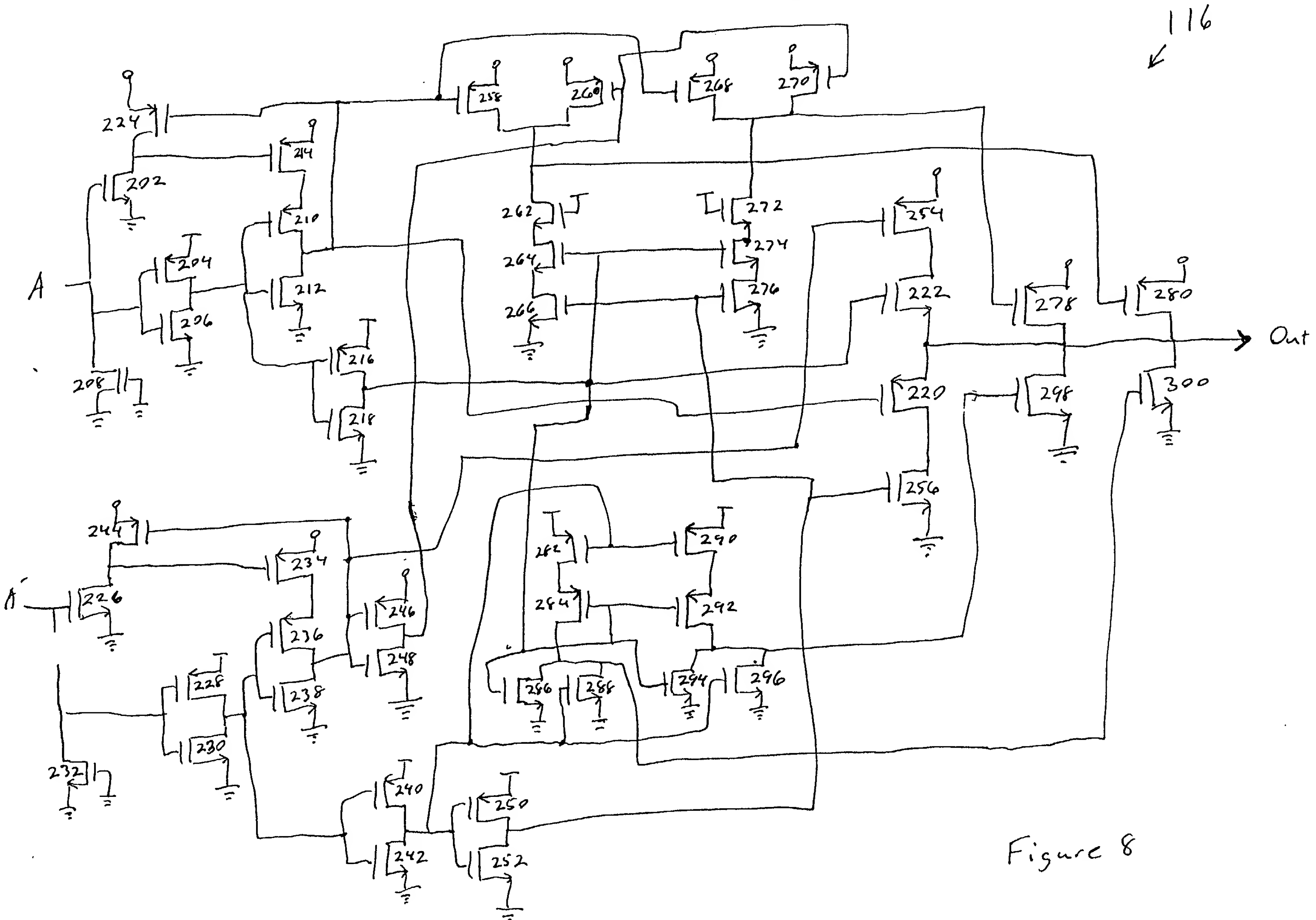

Figure 8

ATTORNEY'S DOCKET NO.
TI - 29632

APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, section 1.56.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: ***INPUT/OUTPUT ARCHITECTURE FOR INTEGRATED CIRCUITS***		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH: **Ronald O. Neerings, Reg. No. 34,227** **Wade J. Brady, III, Reg. No. 32,080** **Jay Cantor, Reg. No. 19,906** **Robby T. Holland, Reg. No. 33,304** **William B. Kempler, Reg. No. 28,228** **Robert N. Rountree, Reg. No. 39,347** **Frederick J. Telecky, Jr., Reg. No. 29,979**		
SEND CORRESPONDENCE TO: ***RONALD O. NEERINGS*** Texas Instruments Incorporated P. O. Box 655474, M.S. 3999 Dallas, Texas 75265		DIRECT TELEPHONE CALLS TO: ***Ronald O. Neerings*** (972) 917-5299
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SIGNATURE OF INVENTOR: X U-Ming Ko	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: X 11/27/00	DATE:	DATE: